REMARKS

Claim Rejections Under 35 U.S.C. § 103

Claims 1-3, 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* (U.S. Patent No. 6,031,757) in view of *James, Jr. et al.* (U.S. Patent No. 6,240,519). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* (U.S. Patent No. 6,031,757) in view of *James, Jr. et al.* (U.S. Patent No. 6,240,519) as applied to claim 1 above, and further in view of *Kynett et al.* (U.S. Patent No. 5,249,158). Claims 6-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Chuang et al.* (U.S. Patent No. 6,031,757) in view of *James, Jr. et al.* (U.S. Patent No. 6,240,519) as applied to claim 1 above, and further in view of *Johnson et al.* (U.S. Patent No. 5,343,437). Applicants respectfully traverse these rejections.

Claims 1, 5, 6, and 8 have been amended to add limitations regarding the protection of the boot blocks from an erase operation. This subject matter can be found in the current specification at paragraphs 0011 and 0012 as well as in other locations. Additionally, claim 6 already had this limitation but more broadly included write prevention as well. Therefore, no new matter has been entered by the current amendments.

Chuang et al. disclose a write protected, non-volatile memory device. *Chuang et al.* describe a sector lock bit and a write protection voltage that provide a corresponding protectable sector. *Chuang et al.* neither teach nor suggest Applicants' invention, as claimed in the amended claims, of authorizing/protecting a boot block from an erase operation. This is not an obvious difference since, in a flash memory device, these operations are performed in completely different manners using different voltages and timing.

James, Jr. et al. disclose a memory device with two boot blocks at one end of a memory address space. *James, Jr. et al.* neither teach nor suggest Applicants' invention as claimed in the amended claims for authorizing/preventing an erase operation to one of a plurality of boot blocks in a flash memory device.

Kynett et al. disclose a flash memory device that that can have a boot block at either end of the address space. However, *Kynett et al.* neither teach nor suggest Applicant's invention as

claimed in the amended claims for authorizing/preventing an erase operation to one of a plurality of boot blocks.

Johnson et al. disclose a memory that has non-volatile and volatile memory banks. *Johnson et al.*, however, neither teach nor suggest Applicants' invention as claimed in the amended claims.

Even if it were obvious to combine the above-cited references as stated by the Examiner, and Applicants maintain that it is not obvious, there is no combination that would teach or suggest Applicants' invention as claimed in the amended claims for authorizing/preventing an erase operation to a boot block in a memory device having a plurality of boot blocks by a protect status bit or a security voltage.

Claim Rejections Under 35 U.S.C. § 112

Claims 1-4 were rejected under 35 U.S.C. §112, first paragraph, because the specification, while being enabling for, "authorizing the write operation to the first boot area if the data is in a first state **or** the security voltage exceeds a predetermined voltage", does not reasonably provide enablement for "authorizing the write operation to the first boot area if the data is in a first state **and** the security voltage exceeds a predetermined voltage".

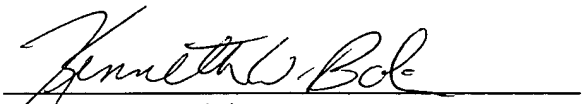
Claim 1 has been amended to overcome the rejection under 35 U.S.C. § 112, first paragraph.

CONCLUSION

For the above-cited reasons, Applicants respectfully request that the Examiner withdraw the Final Rejection and allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date:_____



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